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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
CHUNG, CHI WHAN	

ART UNIT	PAPER NUMBER
2115	3

DATE MAILED: 03/19/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/771,322	SAXENA ET AL.	
	Examiner	Art Unit	
	Chi Whan Chung	2115	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 January 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 - 19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 - 2, 5 - 6, 16 - 18* is/are rejected.

7)☒ Claim(s) *3 - 4, 7 - 15, 19* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claim 1 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

As per claim 1, claim 1 mentions the step of 'determining bit width scaling functions for scaling between different bit-widths.' Function y = f(x) should have dependent variable (y) that is changed by independent variable (x). However, in this part of the claim, it is not clear whether bit-width is the dependent variable or the independent variable of the bit width scaling function. On the other hand, the next step 'determining a normalizing period scaling function to estimate the normalizing period for different bit widths' clearly mentions that the normalizing period is scaled based on different bit widths. Therefore, it is necessary to mention the dependent and independent variables of the bit width scaling function.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1 – 2, 6, and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bogliolo et al., 'Parameterized RTL Power Model for Combinational Soft Macros' (1999), Bhawmik et al., U.S. patent no. 6,463,560, and Matsuo, Koji, Japanese patent no. JP404131970.

5. As per claim 1, **Bogliolo et al.** teach a critical path delay based macro energy model creation method comprising the steps of:

establishing an energy macro table (p. 286 1st col.).

estimating the power consumption for a particular circuit (see the first equation in p. 287).

Bogliolo et al. do not teach the steps of:

determining bit width scaling functions for scaling between different bit-widths; and

determining a normalizing period scaling function to estimate the normalizing period for different bit widths.

Bhawmik et al. teach the steps of:

determining a normalizing period scaling function to estimate the normalizing period for different bit widths (see Fig. 21 and col. 21 lines 18 – 29).

Matsuo teaches the step of:

determining bit width scaling functions for scaling between different bit-widths (see Abstract).

It would have been obvious to one of ordinary skill in the art to combine Bhawmik et al, Bogliolo et al., and Matsuo's methods because Bogliolo et al. provides a motivation for automatic construction of power models for RTL parametric soft-macros using bit-width (p. 284 1st col. 4th paragraph) and Bhawmik et al. and Matsuo teach a way to do so by using scaling functions related to bit-widths so that they can be used to convert values in energy table to power estimation values.

It would have been further obvious to one of ordinary skill in the art to combine these steps because there is no mention that these steps are related to each other.

6. As per claim 2, Bogliolo et al. teach the critical path delay based macro energy model creation method of claim 1 in which said energy macro table comprises a three dimensional table (p. 286 1st col. Section 3.1).

7. As per claim 6, Bogliolo et al. teach the critical path delay based macro energy model creation method of claim 1 wherein a power value is utilized to establish said energy per event table (see Pin in p. 286 1st col. 1st paragraph of 3.1. Pin is the average input signal probability, which is associated with a power value).

8. As per claim 16, it is well known in the art that power = energy / period. Once bit width scaling function and the typical normalization period scaling function are given, it would provide the scaled versions of the energy and the normalized period. Therefore, it would have been obvious to one of ordinary skill in the art to use the values obtained from these functions to get the scaled power values.

9. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bhawmik et al., U.S. patent no. 6,463,560, Bogliolo et al., 'Parameterized RTL Power Model for Combinational Soft Macros' (1999), Matsuo, Koji, Japanese patent no. JP404131970, and Jochens et al., 'A New Parameterizable Power Macro-Model for Datapath Components' (1999).

10. As per claim 5, Bogliolo et al. in view of Bhawmik et al. and in further view of Matsuo teach all of claim 1.

Jochens et al. teach the step of generating energy per event values corresponding to average characteristic parameters for a sample number of varying bit width circuits (see Table 1: Estimation error of the Hd-Model).

It would have been obvious to one of ordinary skill in the art to add this step to the series of steps in claim 1 because there is no mention that this step is related to the previous steps in claim 1.

11. Claims 17, and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bhawmik et al., U.S. patent no. 6,463,560, Takahashi et al., U.S. patent no. 6,523,157, Bogliolo et al., 'Parameterized RTL Power Model for Combinational Soft Macros' (1999), and Chen et al., 'Architectural Level Hierarchical Power Estimation of Control Units' (1998).

12. As per claim 17, Bogliolo et al. teach a power consumption estimation method comprising the steps of:

establishing input values (see the equation in 3.5 and read sections 3.1, 3.2, and 3.3 on p.286); and

performing bit width scaling (see section 3.2 on p. 286).

Bogliolo et al. do not teach the steps of:

calculating the typical clock period;

normalizing toggle rates;

looking up energy per toggle event; and

converting an energy estimate into a power dissipation estimate.

Bhawmik et al. teach the step of:

calculating the typical clock period (see the clock cycles in Fig. 20 A~ H).

Takahashi et al. teach the step of:

normalizing toggle rates (col. 10 lines 24 – 27).

Chen et al. teach the step of:

looking up energy per toggle event (see equation (1) on p. 212);

converting an energy estimate into a power dissipation estimate (see Fig. 2 on p. 212).

It would have been obvious to one of ordinary skill in the art to combine Bhawmik et al., Takahashi et al., Bogliolo et al., and Chen et al.'s steps because there is no mention that these steps are related to each other.

13. As per claim 18, it would have been obvious to one of ordinary skill in the art to label the energy table parameters include bit width, absolute Trin, absolute Trout, and Spin, because they are just labels.

Allowable Subject Matter

14. Claims 3 – 4, 7 – 15, and 19 are objected to as being dependent upon a rejected base claims, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

15. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Gehman et al., patent no. 6,002,878.

Hauck et al., patent no. 6,091,426.

Gaitoonde et al., patent no. 5,940,779.

Sato, patent no. 5,754,435.

Raghunathan et al., pub. no. 2002/0133792.

Eiermann, M., 'Novel Modeling Techniques for RTL Power Estimation' (2002).

Lee, J., 'Power Estimation Using Input/Output Transition Analysis (IOTA)' (1998).

Jochens et al., 'A New Parameterizable Power Macro-Model for Datapath Components' (1999).

Corgnati et al., 'Clustered Table-Based Macromodels for RTL Power Estimation' (1999).

Wu et al., 'Cycle-Accurate Macro-Models for RT-Level Power Analysis' (1998).

Raghunathan et al. 'Register-Transfer Level Estimation Techniques for Switching Activity and Power Consumption' (1996).

Landman et al., 'High-Level Power Estimation' (1996).

Gupta. et al. 'Energy-Per-Cycle Estimation at RTL'

Chou, T., 'Accurate Power Estimation of CMOS Sequential Circuits' (1996).

Bruni D. et al., 'Delay-Sensitive Power Estimation at the Register-Transfer Level' (2001).

Brandolese, C. et al., 'Energy Estimation for 32-bit Microprocessors' (2000).

Lajolo, M. et al., 'Efficient Power Estimation Techniques for HW/SW System'

Garcia, A., 'Cycle-Accurate Energy Estimation in System Level Description of Embedded Systems' (2002).

Kalla, P. et al., 'SEA: Fast power estimation for micro-architectures' (2003).

Bogliolo, A. et al., 'Regression-Based RTL Power Modeling' (July 2000).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chi Whan Chung whose telephone number is (703)305-8788. The examiner can normally be reached on Monday~Friday 9:00am -5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas Lee can be reached on (703)305-9717. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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